VERTICALLY STACKED MEMORY CHIPS IN FBGA PACKAGES

ABSTRACT

A method and structure for a memory structure that includes a plurality of substrates stacked one on another is disclosed. The invention includes a plurality of connectors connecting the substrates to one another and a plurality of memory chip packages mounted on the substrates. The connectors have a size sufficient to form a gap between the substrates. The gap is larger than a height of the memory chip packages.